Claims

What is claimed is:

1. A method of performing digital multi-channel audio signal decoding, said method comprising:

performing analog-to-digital conversion of a composite analog audio signal at a fast clock rate to generate a composite digital audio signal at a first sample rate;

performing digital frequency compensation of said composite digital audio signal at said first sample rate to generate a compensated composite audio signal; and

performing digital channel demodulation and filtering of said compensated composite audio signal at said first sample rate to generate a first single channel audio signal at a second sample rate.

2. The method of claim 1 further comprising performing DBX decoding of said first single channel audio signal at said second sample rate to generate a decoded audio signal at a third sample rate.

3. The method of claim 2 wherein said fast clock rate is greater than said first sample rate, said second sample rate

is less than said first sample rate, and said third sample rate is less than or equal to said second sample rate.

4. The method of claim 2 wherein said fast clock rate is an integer multiple of said first sample rate, said second sample rate, and said third sample rate.

5. The method of claim 2 further comprising performing digital channel demodulation and filtering of said compensated composite audio signal at said first sample rate to generate a second single channel audio signal at said third sample rate.

6. The method of claim 5 further comprising generating a left audio signal and a right audio signal based on said decoded audio signal and said second single channel audio signal at said third sample rate.

7. The method of claim 2 further comprising performing sampling rate conversion of said decoded audio signal to generate a second audio program (SAP) output signal at a standard audio output rate.

8. The method of claim 6 further comprising performing sampling rate conversion of said left audio signal and said right audio signal to generate a left stereo output signal and a right stereo output signal at a standard audio output rate.

9. The method of claim 5 further comprising performing sampling rate conversion of said second single channel audio signal to generate a mono audio output signal at a standard audio output rate.

10. The method of claim 1 wherein said first single channel audio signal at said second sampling rate comprises one of:

a second audio program (SAP) signal; and

a left minus right (L-R) stereo difference signal.

11. The method of claim 5 wherein said second single channel audio signal at said third sample rate comprises a left plus right (L+R) stereo sum signal.

12. The method of claim 1 wherein said performing digital frequency compensation comprises implementing a digital filter compensating for uneven frequency response in said composite digital audio signal due to an uneven frequency response of a previous IF demodulation function.

13. The method of claim 2 wherein said performing DBX decoding comprises implementing a combination of digital filters that are a translation of a set of analog filters.

14. The method of claim 2 wherein said performing DBX decoding includes performing variable de-emphasis of said first single channel audio signal by, in part, indexing into

a look-up-table (LUT) and performing linear interpolation on data samples extracted from said LUT to generate an intermediate coefficient value.

15. A system for performing digital multi-channel audio signal decoding, said system comprising:

a sigma-delta analog-to-digital (A/D) conversion block operating on a composite analog audio signal to generate a composite digital audio signal;

a clock generation block generating clock signals used in said multi-channel audio signal decoding; and

a DSP processing block including a multi-stage pipelined data path performing certain digital multi-channel audio signal processing functions in response to a set of instructions.

16. The system of claim 15 further comprising:

an input buffer block connected between said sigma-delta A/D conversion block and said DSP processing block to transfer said composite digital audio signal to said DSP processing block;

a configuration register block interfacing to at least said DSP processing block, said input buffer block, and said sigma-delta A/D conversion block; and

an output buffer block interfacing to at least said DSP processing block and said clock generation block to output standard audio output signals at standard audio output rates.

17. The system of claim 15 wherein said DSP processing block further includes:

data memory for temporary storage of data;

coefficient memory for storing sets of coefficients used in said digital multi-channel audio signal decoding;

instruction memory for storing said set of instructions; and

an instruction decoder for interpreting said set of instructions.

18. The system of claim 15 wherein said multi-stage pipelined data path comprises:

a memory address calculation stage;

a memory data fetch stage;

a multiplication stage;

an accumulation/mantissa-generation/signal-shifter stage; and

a registers/memory-write stage.

19. The system of claim 15 wherein said set of instructions, operating on said multi-stage pipelined data path, is capable of performing at least:

digital frequency compensation of said composite digital audio signal to generate a compensated composite audio signal at a first sample rate;

digital channel demodulation and filtering of said compensated composite audio signal to generate a first single channel audio signal at a second sample rate;

digital channel demodulation and filtering of said compensated composite audio signal to generate a second single channel audio signal at a third sample rate;

DBX decoding of said first single channel audio signal to generate a decoded audio signal at said third sample rate;

re-matrixing of said decoded audio signal and said second single channel audio signal to generate left and right audio signals at said third sample rate; and

sampling rate conversion of at least one of said decoded audio signal, said left and right audio signals, and said second single channel audio signal to generate at least one standard audio output signal at a standard audio output rate.

20. The system of claim 15 wherein said set of instructions includes:

an instruction for performing first-order IIR filtering in no more than three clock cycles; and

an instruction for performing second-order IIR filtering in no more than five clock cycles.

21. The system of claim 15 wherein said system is implemented as part of an ASIC chip.